

TECHNICAL DESCRIPTION

MARCONI-E.M.I. SYSTEM OF TELEVISION

PART 3. TIMING PULSE GENERATORS

CONTENTS

Item 3.0 . . .	General Principles
Item 3.1 . . .	The Master Oscillator (Types 3a and 3b)
Item 3.2 . . .	The Line Divider (Types 2b and 2c)
Item 3.3 . . .	The Frame Divider (Types 2b and 2c)
Item 3.4 . . .	The Master Oscillator Mains Hold (Type 4a)
Item 3.5 . . .	The Timing Pulse Delay Units
Item 3.6 . . .	The Timing Pulse Distribution Delay Unit (Type 1a)

TIMING PULSE GENERATORS

The various control pulse generators described in Part 2 all require to be energised, as will have been seen, by timing pulses, and it will be noted that a total of three individual timing pulses is required for this purpose. These frequencies are (1) the master frequency of 20250 c/s, (2) the master line frequency of 10125 c/s, and (3) the master frame frequency of 50 c/s. These three frequencies must be rigidly locked together so as to avoid any possibility of mutual phase variation, since this would produce undesirable effects in the picture, such as loss of interlacing. This makes it necessary that these frequencies should not be individually generated, but should be mutually interlinked, either by a system in which the two upper frequencies are produced by multiplication of an initially generated frequency of 50 c/s, or alternatively by a system in which the upper frequency of 20250 c/s is initially generated, the two lower frequencies being divided from it. The second course is preferred, as the precision of timing of the two lower frequencies will clearly be greater, and mutual phase variation will therefore be less.

It is furthermore necessary that the master frame frequency should be held in step with the frequency of the supply mains. Two important advantages result from this. In the first place, A.C. lighting can be used for the scenes which are to be televised, and this is obviously a convenience. When an illuminator is operated from A.C., the light will in theory vary in intensity at 100 c/s. With practical lighting equipment this variation will be very small, as the great thermal hysteresis of the thick filaments employed very largely counteracts such variations. Nevertheless, the flicker cannot be assumed to be entirely zero. Since the light is continuously acting upon the mosaic of the emitron, such flicker will be integrated over the whole of the frame period, and will in general produce no visible effect, or at the worst a very slight horizontal shading over some part of the frame. This would never be noticed in practice. On the other hand, if the frame frequency were not the same as the mains frequency, then the bar of horizontal shading produced by any small variation in light intensity in the illuminators would move up or down, and by virtue of its movement would be visible. The second advantage of locking the mains and frame frequencies is that the specification for H.T. smoothing in receivers in the system generally can be less stringent. Taking for example the case of the home receiver, H.T. is derived by a mains rectifier, and if the smoothing is not ideal there will be a trace of hum in the cathode ray tube beam supply. The hum will have a frequency of 100 c/s, and will produce a faint bar of horizontal shading on the tube screen. If the frame and mains frequencies are locked at the transmitting end, and if it may be assumed that the mains frequency at the receiving end is locked to that at the transmitting end,

the horizontal shading bar will remain fixed in position and since in any case it will have a very small intensity it will be to all intents and purposes invisible. If, however, the frequency is not locked, the bar will move up or down, and it will then be noticeable and possibly objectionable. It may correctly be argued that this is an effect which should logically be corrected by the employment of adequate smoothing in the receiver H.T. supply, but the additional cost of the smoothing necessary to remove the last trace of hum would be considerable and would appreciably affect the cost of receivers. Therefore, since there is no great difficulty in locking the mains and frame frequencies, this course is undoubtedly to be preferred.

The arrangements for locking the two frequencies require careful consideration, for the following reason. The mains frequency to which the frame frequency will be locked cannot be guaranteed to be absolutely constant, and the transmitted frame, line and master frequencies will therefore be subject to slight variations. Now the receivers may be either electrical or mechanical, and the chief difference between the two types is that the inertia of the scanning mechanism of an all-electrical receiver is negligible, but that of a mechanical receiver is not negligible. In an entirely electrical receiver such as one employing a cathode ray tube for the reproduction of the picture, the scanning mechanism, being electrical, can instantly respond to any slight change in the received line and frame frequencies. A mechanical receiver, on the other hand, will contain a mechanical scanning system of appreciable inertia, which requires a small but definite time to readjust itself to any change in the received line and frame frequencies. Should these frequencies change slowly a mechanical system will be able to follow them and keep the picture in synchronism, but if the frequencies change rapidly from one value to another, then in the interval required by the inertia of the mechanical system to adjust itself to the new frequencies the picture will be partially or wholly out of synchronism in the line or frame directions, and temporary distortion will result. For the benefit of mechanical receivers, therefore, we must arrange that the device which locks the frame and mains frequencies is not instantaneously operative, so that if the mains frequency suddenly departs from its previous value, the frame frequency will be brought into step gradually. In these circumstances, receiver scanning mechanisms of appreciable inertia will be able to follow the slow change in line and frame frequencies and temporary lack of synchronism will be avoided. This point has been taken into account in the timing pulse generating system which is now to be described.

The underlying principles of operation of the system are as follows. The master frequency is generated at 20250 c/s by a *Master Oscillator*, and the output from this unit is available to trip all control pulse generators

TIMING PULSE GENERATORS

Technical Description

M-E.M.I. System of Television

Item 3.0. April, 1939

requiring the master frequency. This master frequency is also applied to a further unit known as the *Line Divider*, which divides it by 2, giving the line frequency of 10125 c/s, which is then supplied to all generators requiring line frequency. A further output from the Master Oscillator is applied to a unit termed the *Frame Divider*, which divides it by 405, and therefore provides a master frame frequency of 50 c/s, which is again supplied to those generators which require it.

The three fundamental frequencies are now available, but are not yet locked to the mains frequency. To do this a supply of the master frame frequency is mixed with an output of the mains, and the mixture is then rectified. Should the two frequencies differ, the rectified output will contain the difference frequency. This difference frequency is then employed to drive a synchronous motor whose shaft controls a variable condenser acting upon the Master Oscillator frequency. Since the Frame Divider links the master and master frame frequencies by a factor of 405, any change in the master frequency will be reproduced in proportionate degree in the master frame frequency. The sense of the operation of the variable condenser by the motor is, of course, arranged so that if for example the mains frequency increases, the motor will increase the master frequency, and via the Frame Divider the master frame frequency will in turn increase.

The synchronous motor which drives the Master Oscillator condenser must, of course, be self-starting, and also must be capable of smooth and steady operation. Both these considerations require that it should be of the 3-phase type. The difference frequency which operates it must therefore be a 3-phase difference frequency. Such a frequency can be produced by combining (1) normal, i.e. single phase frame frequency from the Frame Divider with a 3-phase output from the mains, or (2) by deriving from the single phase frame frequency emanating from the Frame Divider a 3-phase frame frequency, and combining this with a single phase output from the mains. Apparatus employing the first of these methods has been constructed, and operates very satisfactorily, but 3-phase mains must be available. This type is therefore quite suitable for a fixed installation such as that at the London Television Station. However, 3-phase mains cannot always be found at the sites of outside broadcasts where similar apparatus is naturally required, and in this case the second type is preferable. Even if 3-phase mains are available there is, however, no objection to using the second type, and this has consequently been standardised for outside broadcast units and the London Television Station. Only this type will therefore be described.

The apparatus which effects the preparation of the difference frequency for application to the synchronous motor is known as the *Master Oscillator Mains Hold*.

The three master pulses, after generation by the above apparatus, must now be distributed to the various control pulse generators which require them, and in this connection two sets of circumstances may arise. (1) The master pulses may be required to time only one set of control pulse generators, as for instance obtains in the O.B. unit. In this case no additional problem is involved. (2) They may be required to time simultaneously more than one set of control pulse generators, as for instance at the London Television Station, where the control pulse generators of all the studios are simultaneously timed by a single set of master pulses supplied from the Central Control Room. In this case the time of arrival of the equivalent pulses at each studio will be different in each case in view of the different lengths of connecting cable. This in itself does not cause any difficulty unless it is desired to mix the outputs of two studios in the course of a multi-studio presentation. In this case the studio apparatus must be tripped at precisely the same moment, as otherwise the individual synchronising pulses from the two studios which are being mixed will not be mutually in synchronism, and the picture will 'judder.' To avoid this, circuits termed the *Timing Pulse Distribution Delay Networks* are provided at the point where the timing pulses are generated, so that the time of arrival of the pulses at the various studios can be equalised. The networks are, of course, inserted in the pulse outputs to all of the studios except the most distant one, so that the transmission time of the quicker path is lengthened so that it equals that of the longest path. Such networks are required for the master frequency and master line frequency, but not for the frame frequency, where the difference in transmission time is too small to produce any effect.

When the three sets of timing pulses have arrived at a set of control pulse generators, a complicated problem arises in that the various units of the control pulse generator, such as the keystone generator, the black-out generator, etc., do not all require to be timed in absolute synchronism for reasons connected with the transmission time of pulses and vision signals through the camera and picture channels. A somewhat complex system of both fixed and variable delay networks is required, and these are associated partly with the timing pulse inputs to the control pulse generators, and partly with the camera channels. These circuits can be best understood, however, if considered collectively, and they are therefore described in this section under the heading *The Pulse Delay Units*.

The following apparatus will now be described in order :—

The Master Oscillator, under Item 3.1.

The Line Divider, under Item 3.2.

The Frame Divider, under Item 3.3.

The Master Oscillator Mains Hold, under Item 3.4.

The Timing Pulse Delay Units, under Item 3.5.

The Timing Pulse Distribution Delay Networks, under Item 3.6.

THE MASTER OSCILLATOR—TYPES 3a & 3b

The circuit of this apparatus is illustrated in Fig. 1.

The valve V_1 constitutes a sinusoidal oscillator generating sine waves at a frequency of 20250 c/s. The circuit is in fact that of a Hartley oscillator, but may not be immediately recognised as such owing to the fact that the anode is effectively earthed by means of the condenser C_1 . The lower end of the inductance L_1 is, however, also earthed, so that this coil is in fact connected between anode and grid with a centre tap connected to the cathode. It will be seen therefore that the circuit only differs from the conventional Hartley circuit in that in the latter the cathode is usually earthed, while the anode and grid are free to oscillate, but in this case the anode is earthed, the grid and cathode being free to oscillate. The tuned circuit which determines the frequency of oscillation is formed from the inductance L_1 and the capacities C_2 and C_3 , of which C_3 is variable and constitutes the means for adjustment of frequency. It is mounted on a spindle of the synchronous motor M , and is therefore automatically controlled by the difference frequency generated by the Master Oscillator Mains Hold unit. The shaft is, however, brought out to the front of the panel in the form of a pointer moving over a scale, so that the setting of the condenser can be observed, and the pointer is constructed so as to be suitable for manual adjustment if necessary. The grid resistance of V_1 is in this circuit placed between the cathode and the centre tapping of L_1 , and is shown as R_1 . In this position it also serves to provide automatic grid bias to the extent of some $-5V$, which retains the operating point of the valve upon the most suitable part of its characteristic, and avoids excessive dissipation.

Since the Line and Frame Dividers and all Control Pulse Generators taking the master frequency pulse require a square topped pulse, the initial sine wave generated by V_1 must be converted into this form. This is carried out by V_2 . The output from V_1 , having an amplitude of about 100V D.A.P., is applied to the grid of V_2 through the series resistance R_2 . The cathode of V_2 is directly earthed, and therefore has no automatic bias. Since the grid of V_2 is also returned via R_2 and L_1 to earth, its standing potential, about which the input from V_1 operates, is that of earth, and the grid-cathode potential is therefore zero. The input from V_1 attempts to drive the grid of V_2 alternately 50V positive and 50V negative with respect to earth. When the grid becomes a volt or two positive, however, the grid-cathode impedance, as is usual with almost all valves, drops to a very low figure owing to grid current, and forms with the resistance R_2 a potentiometer in which the grid is tapped well down. It follows that only a minute fraction of the amplitude of the input sine wave reaches the grid, whose potential remains during the positive half cycle very little above that of earth. Thus, the positive half cycle of the sine wave has been flattened, and therefore

MASTER OSCILLATOR
 Technical Description
 M-E.M.I. System of Television
 Item 3.1. April, 1939

rendered square topped. The negative half cycle now commences, the grid ceases to draw grid current, and the grid-cathode impedance becomes so high that the presence of the resistance R_2 may be neglected. The screen voltage of this valve is quite low, so that it has a short grid base, and the greater part of the negative half cycle on the input sine wave maintains the valve well beyond cut-off. No anode current therefore flows during this period, and the anode potential remains steadily at the potential of the H.T. positive line. Thus, at the anode the part of the cycle corresponding to the negative half cycle of the sine wave applied to the grid has been flattened and therefore rendered square topped. It will be seen, therefore, that if the waveform on the grid is examined by the Waveform Monitor, the flattening of the positive half cycles due to grid current will be seen, but the negative half cycles will be sinusoidal since they are not flattened by grid current action. The positive half cycles at the grid, already flattened, will be reproduced at the anode as negative flattened half cycles, while the negative half cycles of sine wave at the grid will appear at the anode as positive flattened half cycles due to anode current cut-off.

The square topped master frequency output from the anode of V_2 is applied to the grids of both V_3 and V_4 , which form a pair of separate output stages, V_3 feeding master frequency to the Line and Frame Dividers via the output terminals 81, while V_4 supplies master frequency to one or more sets of Control Pulse Generators. The anode circuit contains the output transformer TR_1 , which is parallel fed by the inductance L_2 and the condenser C_8 . The primary is damped by means of the resistance R_3 . The secondary winding 1-4 supplies the output via terminal 82. The circuit is designed to feed a maximum of four sets of Control Pulse Generators simultaneously, each set being fed via a concentric line of 110 ohms impedance. The output lines are all fed in parallel. Since for minimum distortion the optimum load impedance for the pentode V_4 is, as usual, critical, the impedance presented to it from the primary of TR_1 should be constant. This impedance, however, depends upon the number of lines which have been paralleled across the secondary. It is arranged, therefore, that the load impedance will have its optimum value when the impedance across the secondary is that of the maximum number of permissible output circuits in parallel, viz., $110/4 = 27.5$ ohms. If the apparatus is only required to supply one line, then the impedance across the transformer secondary is 110 ohms. This must be reduced to the correct value by the connection of a parallel resistance shown as R_4 and having a value of 37 ohms (6W). If the apparatus is to feed two lines, their combined impedance will be 55 ohms, and R_4 must be 55 ohms (5W). Similarly, for three lines, R_4 must be 110 ohms (3W). (When R_4 is 37 ohms the oscillator is known as *Type 3a*, and when R_4 is absent it is known as *Type 3b*.)

The anodes and screens of the various valves are decoupled, fed and metered normally.

The synchronous motor M has 3^{ph} windings set at mutual angles of 120° , and a rotating field is therefore generated when 3-phase current is applied to the stator windings. For the motor to be truly synchronous, the rotor must be polarised with a steady field. This can, of course, be done by providing a single rotor winding fed with steady D.C., but a simplification has been effected by incorporating a permanent magnet in the rotor for polarisation. In operation, if the frequency of the Master Oscillator is exact, no current will be applied to any of the stator windings by the Master Oscillator Mains Hold, but if the frequency is incorrect, a 3-phase current in either one direction or the other will be applied to the stator windings, and the rotating field so produced will attempt to drag the steady rotor field, due to the polarising magnet, round with it. The shaft will therefore rotate and adjust the variable condenser C_3 until the frequency has been restored to the correct value, in which circumstances the 3-phase current for the Master Oscillator Mains Hold will drop to zero, and there will again be no input to the stator windings. The rotor will accordingly remain stationary in the new position.

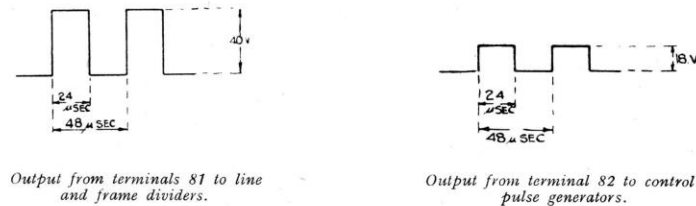


Figure 2

Operation and Maintenance

No monitoring jacks are provided, but the waveform at both outputs (terminals 81 and 82) should appear as in Fig. 2.

In normal operation the following voltage and current readings should be obtained.

Valve	Anode Current	Voltage at Anode Decoupling Point	Screen Voltage
V_1	2mA	90V	—
V_2	15mA	220V	120V
V_3	6mA	200V	100V
V_4	60mA	260V	260V
Total anode feed from 300V line	..	90mA	
Total anode feed from 150V line	..	15mA	

MASTER OSCILLATOR
 Technical Description
 M-E.M.I. System of Television
 Item 3.1. April, 1939

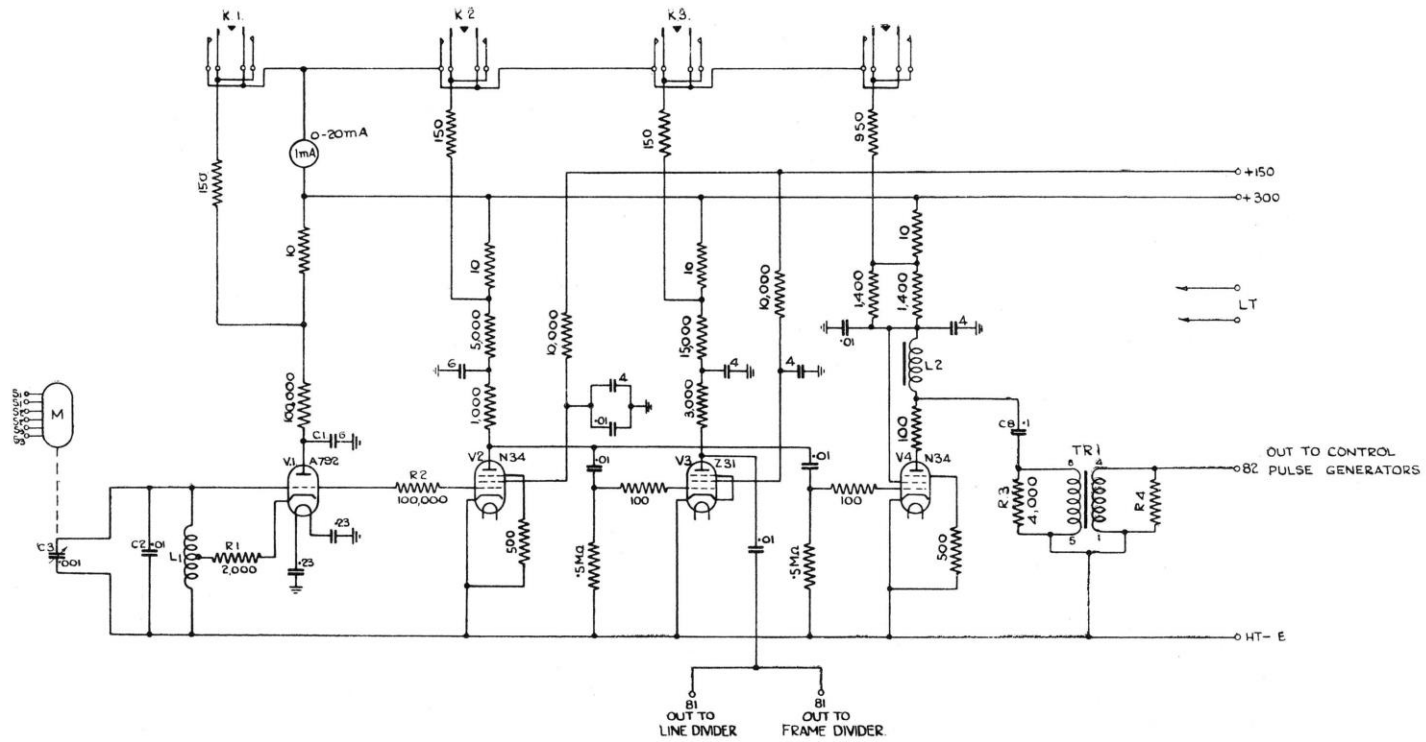


Figure 1. Master Oscillator Circuit.

THE LINE DIVIDER—TYPES 2b & 2c

The function of the Line Divider is to divide by a factor of 2 the master frequency of 20250 c/s, thereby generating the master line frequency of 10125 c/s, consisting of narrow square topped pulses about 3 to 5 micro-seconds wide. The circuit is shown in Fig. 1.

The grid of V_1 is returned directly to the cathode by the grid resistance R_1 , so that there is therefore no grid bias, and the grid-cathode potential is zero. In the absence of any input therefore, the valve is drawing considerable anode current. The anode circuit contains the large anode resistance R_2 , so that the anode potential is consequently very low, its value being +3V. An input at master frequency derived from the valve V_3 of the Master Oscillator, via output terminal 81 of that unit, is applied to the grid of V_1 . The first positive half cycle of this input attempts to drive the grid positive with respect to the cathode, but fails to do so since D.C. restoration takes place, and a negative charge equal in amplitude to the pulse is drawn on to the grid, and stored by the grid condenser C_1 . When the pulse retreats, this negative charge biasses V_1 beyond cut-off, and the anode voltage rises sharply to approximately 300V, the potential of the H.T. line. This positive anode pulse is applied to the series circuit composed of the condensers C_2 , C_3 and C_4 and the diode D_2 . The diode D_2 conducts, and the three condensers are charged to potentials depending inversely upon their capacities. Neglecting C_4 , whose capacity is comparatively large, and noticing that the capacity of C_3 is 10 times that of C_2 , the potential between the upper side of C_3 and earth will be approximately 1/10th of that between the anode of V_1 and earth, i.e. 30V, the remaining 270V existing across C_2 . When the next positive cycle of the input master frequency pulse occurs at the grid of V_1 , the anode voltage drops to a very low value, and but for the presence of D_2 the three condensers would discharge and there would be no resultant effect. Since, however, D_2 cannot conduct in the cathode-anode direction, the condensers C_3 and C_4 do not discharge and the potential of +30V is stored across them. Similarly a potential of +270V is stored across the condenser C_2 , but this must be removed, as we wish to repeat the process of placing an increment of charge upon the condensers C_3 and C_4 , and unless we first discharge C_2 , the total potential stored by C_2 , C_3 and C_4 in series being 300V, would exactly oppose the pulse at the anode of V_1 , and it will not be possible to force any further charge into C_3 C_4 . The diode D_1 is therefore provided with its anode connected to earth and its cathode connected to C_2 , and when the pulse at the anode of V_1 retreats, and the anode potential of V_1 falls to a very low figure, C_2 can clearly discharge through the anode-cathode paths of V_1 and D_1 in series.

LINE DIVIDER

Technical Description

M-E.M.I. System of Television

Item 3.2. April, 1939

The position now is that the effect of one cycle of the input of master frequency has been to store up a voltage of +30 across the condensers $C_3 C_4$. During the second cycle of master frequency the condensers C_2, C_3 and C_4 are again charged as before, and a further increment of nearly +30V is added to the existing charge across $C_3 C_4$, the total charge now being nearly +60V. The upper side of C_3 is connected to the grid of V_4 , and the cathode of this valve receives a permanent positive bias of +47V from the junction of R_5 and R_6 on the H.T. potentiometer $R_3 R_4 R_5 R_6$. Ordinarily, therefore, the grid-cathode potential is -47V, and the valve does not conduct. When the first increment charge is placed on the condensers $C_3 C_4$ in the manner described above, the grid-cathode potential of V_4 is reduced to -17V, but it is still beyond cut-off, and does not conduct. When two such increments have accumulated across $C_3 C_4$, the grid-cathode potential is about +10V and the valve conducts.

The anode circuit contains the anode resistance R_7 , so that when the valve conducts a negative voltage pulse will appear at the anode.

The screen, control grid, and cathode of the valve V_5 from a triode, which co-operates with the further triode V_6 to form a multivibrator. These valves therefore, if supplied with a timing pulse at a certain frequency, will generate a square topped wave at that frequency. The screen of V_5 is directly connected to the anode of V_4 , and their anode resistance R_7 is common. The negative pulse at the anode of V_4 therefore trips the multivibrator $V_5 V_6$, and a square topped pulse is generated. The anode of the valve V_5 has no part whatever in the multivibrator action, but is connected to the upper side of the condenser C_3 . When V_5 is tripped, the anode-cathode path becomes conductive and the condenser C_3 is discharged. The whole of the circuits associated with the valves V_1 to V_6 are now as they were at the beginning. During the cycle that has been described, two pulses at master frequency have occurred. The only effect of the first was to place a certain charge upon C_3 , but the effect of the second was to augment this charge to a value where, via the agency of the circuits associated with V_4 , it would trip the multivibrator $V_5 V_6$. Clearly therefore the multivibrator generates one pulse for every two pulses at master frequency, and the arrangement therefore divides this frequency by 2. The constants of the grid and anode circuits of the multivibrator are so chosen that the square topped pulse will be of the order of 3 to 5 micro-seconds in width, and in the positive sense at the anode of V_6 .

The output from the anode of V_6 is applied to the final valve V_7 , which is an output stage. This valve is a straightforward amplifier, the output being taken from the anode circuit by means of the transformer TR_1 , while the elements $R_8 C_5$ provide automatic grid bias. As in the case of the second output of master frequency from the Master Oscillator, the output from the secondary of the transformer TR_1 may be required to feed from 1 to 4 outgoing lines in parallel, each of 110 ohms characteristic impedance. The

transformer is therefore designed to work into a load impedance of four 110 ohm lines in parallel, viz., 27.5 ohms, but if less than the maximum number of lines are being used, the resistance R_9 must be inserted to bring the resultant impedance to this figure. This is exactly the same as the arrangement used in the Master Oscillator, and as before if the apparatus is to feed one line, R_9 must be 37 ohms (6W); for two lines it must be 55 ohms (5W), and for three lines, 110 ohms (3W). (When R_9 is present and has a value of 37 ohms, the Divider is known as *Type 2b*. When it is absent it is known as *Type 2c*.)

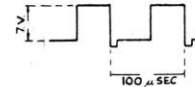


Figure 2
The Process of Division as seen at the Jack J1

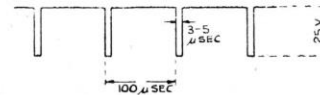


Figure 3
Waveform of the Master Line Frequency at the Jack J2

Operation and Maintenance

The jack J_1 enables the process of division to be examined on the Waveform Monitor, the D.C. jack of which must be used to avoid upsetting the capacity across J_1 . At this jack the appearance of the waveform should be as shown in Fig. 2. The master line frequency output may be observed on the jack J_2 , and its appearance, when the total load across the secondary of the transformer TR_1 is 27.5 ohms, should be as in Fig. 3.

The amplitude of the input to the grid of V_1 should be 40V of master frequency pulses.

During normal operation the following voltage and current readings should be obtained:

Valve	Cathode Current	Voltage at Anode Decoupling Point	Screen Voltage	Cathode Voltage
V_1	14.5 mA	290V	100V	—
V_4	—	240V	—	47V
V_5	1 mA	—	240V	—
V_6	9.5 mA	250V	—	—
V_7	9 mA	285V	130V	2V
Total anode feed from 300V line ..			25mA	
Total anode feed from 150V line ..			15mA	

THE FRAME DIVIDER—TYPES 2b & 2c

The function of the Frame Divider is to divide the master frequency by a factor of 405, and thereby generate the master frame frequency of 50 c/s, consisting of narrow square topped pulses some 200 micro-seconds wide. The division cannot be accomplished in one stage, but takes place in three stages. The first stage divides the master frequency by a factor of 5, and thus generates a pulse of 4050 c/s. The second stage divides this intermediate frequency by 9, producing a frequency of 450 c/s, and the third stage divides this second intermediate frequency by 9, generating therefore the final master frame frequency of 50 c/s. The circuit is shown in Fig. 1.

The grid of V_1 is returned directly to the cathode by the grid resistance R_1 , so that there is therefore no grid bias, and the grid-cathode potential is zero. In the absence of any input therefore, the valve is drawing considerable anode current. The anode circuit contains the large anode resistance R_2 , so that the anode potential is consequently very low, its value being +15V. An input at master frequency derived from the valve V_3 of the Master Oscillator, via output terminal 81 of that unit, is applied to the potentiometer R_{18} R_{19} , from the junction of which the pulses, reduced to $\frac{1}{3}$ of their original amplitude, are applied to the control grid of V_1 . This reduction in amplitude is required by the operating characteristics of V_1 . The first positive half cycle of this input attempts to drive the grid of V_1 strongly positive with respect to its cathode, but fails to do so. The reason for this is that owing to the absence of grid bias, grid current is drawn and D.C. restoration occurs, a negative charge equal in amplitude to the amount by which the pulse would otherwise drive the grid-cathode potential positive being drawn on to the condenser C_1 and stored there. When the first negative half cycle of the master frequency input occurs, this, together with the negative charge on C_1 , biasses V_1 beyond cut-off, and its anode potential rises to the value of its effective H.T., which is +250V. This positive anode potential of +250V is applied to the circuit composed of the condenser C_2 , the diode D_2 and the condenser C_3 in series. The diode D_2 conducts, and C_2 and C_3 are charged to potentials which are inversely proportional to their capacities. The actual potential across C_3 at this moment is +5V, and that across C_2 is +245V. The next positive half cycle of the master frequency input now occurs, and the anode potential of V_1 is driven down to +15V. But for the presence of the diode D_2 , the condensers C_2 and C_3 would both discharge, but no current can flow out of C_3 from the cathode to the anode of D_2 , so that the charge of +5V is stored in the condenser C_3 . As will be seen later, we shall add a further increment of charge to C_3 , but this will be impossible if the anode voltage of V_1 , which is to produce this charge, is opposed by the charge of +245V which is still held in C_2 . The

additional diode D_1 is therefore provided, with its anode connected to earth and its cathode to C_2 , so that during the second positive half cycle of the master frequency input C_2 discharges via the anode-cathode paths of V_1 and D_1 in series, as soon as the anode potential of V_1 has been driven down to +15V. During the second negative half cycle of the master frequency input, the anode potential of V_1 rises as before to +250V, and this pulse again charges the condensers C_2 and C_3 in series. This is possible since this potential of +250 is only opposed by the small charge of +5V still held on C_3 . The anode potential of V_1 , as before, divides itself between C_2 and C_3 in the inverse ratio of their capacities. Therefore, to the original charge of +5V on C_3 there is now added a further charge, which, of course, cannot again be exactly +5V but which will be a minute fraction under this figure. Neglecting this error, however, the charge from C_2 has risen after this second stroke to +10V. The next positive cycle of the master frequency input now occurs, the anode potential of V_1 falls to +15, the diode D_2 as before prevents any of the charge on C_3 flowing out of this condenser, and D_1 discharges C_2 in preparation for the next stroke. Every complete cycle at master frequency therefore steps up the potential on C_3 by approximately +5V, and after five such cycles the potential across C_3 will be approximately +25V. It will be seen from Fig. 1 that this potential across C_3 is applied to the grid of V_3 through the secondary winding 3-4 of the transformer TR_1 , so that the grid-earth potential has been mounting step by step as each increment of charge has been added to C_3 . The cathode of V_3 , however, receives a bias of +29V derived from the potentiometer R_5 , which is part of the H.T. potential divider R_3 R_4 R_5 R_6 . It will be seen, therefore, that at a time when no charge has been placed upon C_3 , the grid-cathode potential is -29V, and the valve does not conduct. Further, the characteristics of the valve are so chosen and arranged that even when four increments of charge have been placed on C_3 , the grid-earth potential being then +20V and the grid-cathode potential being -9V, there is still no conductivity. The fifth increment, however, raises the grid-earth potential to +25V and reduces the grid-cathode potential to -4V, and the screen and anode paths now conduct. Current commences to flow in the primary winding 1-2 of the transformer TR_1 . The flux so generated induces a voltage in the secondary winding 3-4 in such a sense as to augment the positive potential of the grid still further. This in turn induces more screen current, and this again more positive grid potential. The action is rapidly cumulative, a strong positive pulse being applied to the grid from the secondary winding 3-4. This pulse is of considerable amplitude, and attempts to drive the grid-cathode potential to a considerable positive value.

FRAME DIVIDER

Technical Description

M.-E.M.I. System of Television

Item 3.3. April, 1939

As usual, however, this cannot occur since the moment the grid-cathode potential exceeds zero, restoration of D.C. occurs and a negative charge equal in amplitude to the amount by which the grid-cathode potential desires to exceed zero is drawn on to the grid and placed upon the condenser C_3 . The grid-cathode potential therefore remains at zero. After a time, due to saturation, the screen current of V_3 can increase no more, the current in the primary winding 1-2 is momentarily stationary, and no flux cuts across the secondary winding 3-4. The positive pulse which this winding was applying to the grid of V_3 therefore ceases, and the voltage across the condenser C_3 (which is, of course, the grid-earth potential) is the original +25V, placed there by the five small charges, together with a large negative voltage due to D.C. restoration at the time that the grid of V_3 was drawing grid current. This negative charge is much greater than the original positive charge of +25V, and the potential on the upper side of C_3 is therefore considerably negative with respect to earth. This negative potential, together with the automatic grid bias of +29V from R_5 , biases V_3 beyond cut-off. In passing from the fully conductive state to the non-conductive state the screen current of V_3 must fall from its former high value to zero. This decrease of current flowing in the primary winding 1-2 of TR_1 now induces in the secondary winding 3-4 a potential which tends to drive the grid negative. We have already seen that in any case the grid is becoming negative owing to the charge placed upon C_3 by D.C. restoration, and that this is greater than the original positive charge of +25V. It is, however, driven even further negative by this new negative pulse from the secondary of TR_1 . Finally, the screen current falls to zero, and there is now no current in the winding 1-2 and no flux in the transformer and this additional negative pulse ceases. If no action had meanwhile taken place we should be left with a resultant negative potential at the grid of V_3 due to the excess of the negative potential on C_3 due to D.C. restoration over the original charge of +25V. We observe, however, that while the diode D_2 cannot discharge to earth potentials on the upper side of C_3 which are positive to earth, it is conductive to potentials which are negative to earth. The negative charge on C_3 therefore discharges via the cathode-anode path of D_2 and the cathode-anode path of D_1 in series. There is now no potential across C_3 , and the state of the circuit is exactly that which obtained before the first cycle of the original master frequency input appeared on the grid of V_1 . It will be seen that for five master frequency pulses we have obtained one pulse of anode current in the valve V_3 , so that the circuits associated with V_1 , V_2 and V_3 have divided the original frequency by 5, and the anode current of V_3 will pulse at a frequency of 4050 c/s.

It will be noticed that between the anode of D_1 and earth there is included the resistance R_7 . This resistance is not essential to the operation of the circuit as a divider, but it is essential in order that the process of division may be inspected and an adjustment made if necessary to obtain the correct

divisor. During every positive half cycle at master frequency, when the anode potential falls to +15, the large potential across C_2 is discharged by the diode D_1 . The current in this diode passes through R_7 , across which therefore a short pulse will appear at each such discharge. Referring to Fig. 2, these pulses are shown at *A*. At the end of each period of five master frequency pulses when V_3 becomes conductive and subsequently the diodes D_1 and D_2 in series discharge the negative potential across C_3 , there will be a further pulse across R_7 , since the current due to this discharge must also pass through this resistance. These pulses are shown in Fig. 2 at *B*. Their shape is what would be expected from the action of the circuit as described above. The initial sharp rise in the negative sense is due to the rapid increase of current through D_1 , D_2 and R_7 produced by the appearance at the grid of the sharp negative voltage pulse from the secondary of TR_1 , consequent upon the rapid fall in the screen current. The subsequent decay of the pulse corresponds to the exponential discharge of the total negative potential across C_3 , including that due to D.C. restoration, through D_1 , D_2 and R_7 . It will also be noticed that the amplitude of the five pulses *A* steadily decreases, so that a line drawn through their negative peaks has a saw-toothed configuration. This is because the voltage across C_2 is progressively less, each time it is discharged, by the amount of the voltage then existing across C_3 . Clearly, the voltage to be discharged after the first step is 245, after the second 240, after the third 245, after the fourth 230, and after the fifth and last step 225.

For convenience in observation, the jack J_1 is connected across R_7 , and the appearance of the waveform when examined by the Waveform Monitor is as shown in Fig. 2. It will be realised that the pulses *A* have the frequency of the original master frequency, but the frequency of the pulses *B* is that of the divided frequency. Should the automatic grid bias of V_3 provided from the potentiometer R_5 be excessive, then it may be that six increments of charge will be necessary to bring about conductivity in V_3 , and the pulses *B* will be separated by six instead of five pulses of the *A* type. If the cathode potential from R_5 is too low, then four increments might be enough to activate the valve V_3 . The divisor may clearly be ascertained by observing the number of *A* pulses which occur between every pair of *B* pulses, and the potentiometer R_5 is set so that there are five *A* pulses between a pair of *B* pulses. The potentiometer R_5 is brought out as a preset manual control designated $\div 5$. The resistance R_7 tends to slow up the discharge of C_3 and elongate unduly the pulses *B*. This effect is reduced by shunting it with the condenser C_7 .

The valve V_3 is, we have seen, alternately fully conductive and non-conductive at the original master frequency. By providing V_3 with a large anode resistance, R_8 , it will clearly serve as the initial valve, that is to say, the valve corresponding to V_1 , of a further stage of division. It is accordingly

FRAME DIVIDER
 Technical Description
 M-E.M.I. System of Television
 Item 3.3. April, 1939

arranged that V_3 , V_4 and V_5 constitute a second stage of division operating precisely as does the first, but having a divisor of 9. The first increment is, as before, +5V, but they become progressively less, and the final positive potential across C_3 is of the order of 40V. Accordingly the cathode potentiometer R_9 is in this case set to give a bias of some 45V. This potentiometer is brought out to a preset manual control designated $\div 9$. The anode current of V_5 therefore pulses at the second divided frequency of 450 c/s, and this valve, together with V_6 and V_7 , form a third stage of division similar to the second, which effects a further division by 9. Again the cathode potentiometer R_{10} is brought out to a preset manual control designated $\div 9$. The output from V_7 is applied to the two separate output stages V_8 and V_9 , V_8 being provided to feed the Master Oscillator Mains Hold unit, and V_9 to feed all Control Pulse Generators requiring master frame frequency. The amplitude of the master frame frequency pulses at the anode of V_7 is far too great to be applied directly to the grid of V_8 , so the anode resistance of V_7 is composed of the two elements R_{11} and R_{12} , which form a potentiometer at the junction of which a suitable amplitude is found. This is applied to the grid of V_8 , and appears amplified and reversed in its anode circuit. An output is taken via the blocking condensers C_4 and C_5 and the isolation resistance R_{13} to the terminal 81 for application to the Master Oscillator Mains Hold apparatus. The pulses are here in the positive sense, and have a width of some 200 micro-seconds and an amplitude of some 20V.

The pulses may be monitored by the jack J_4 , at which they have an amplitude of 5V. The pulses at the anode circuit of V_8 are also applied to the control grid of V_9 , which is a pentode output stage embodying the output transformer TR_2 , which is parallel fed by the resistances R_{14} , R_{15} , R_{16} and the condenser C_6 . The secondary of the transformer is designed to feed master frame frequency pulses to a maximum of four sets of Control Pulse Generators, which are connected to it by four 110 ohm lines in parallel. The secondary load impedance must be maintained constant, as the impedance referred to the anode circuit of the pentode V_9 should, of course, be the optimum load impedance of the valve. The transformer is therefore designed for a fixed secondary load impedance of four 110 ohms lines in parallel, viz, 27.5 ohms, and if it is not required to feed the full number of lines a resistance R_{17} must be provided of such a value that the resultant impedance will be 27.5 ohms. If one line is being fed, R_{17} will be 37 ohms, for two lines 55 ohms, and for three lines 110 ohms. (When R_{17} is present and has a value of 37 ohms, the Frame Divider is known as *Type 2b*. If it is absent, it is known as *Type 2c*.)

The sense of the master frame frequency across the transformer secondary is negative, and its amplitude 20V.

Operation and Maintenance

In operation the three potentiometers R_5 , R_9 and R_{10} are set so that the waveform appearing at the jacks J_1 , J_2 and J_3 are as shown in Figs. 2, 3 and 4. The final output at master frame frequency when examined at the jack J_4 should appear as in Fig. 5.

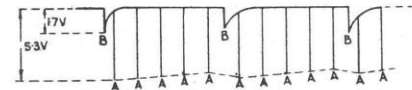


Figure 2
 Waveform of 1st Divider
 ($\div 5$) at the Jack J1

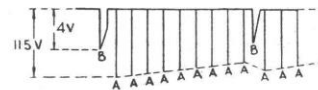


Figure 3
 Waveform of 2nd Divider ($\div 9$)
 at the Jack J2

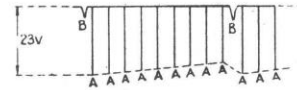


Figure 4
 Waveform of 3rd Divider ($\div 9$)
 at the Jack J3

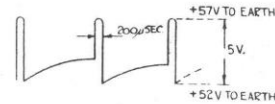


Figure 5
 Waveform of Master Frame Frequency
 at the Jack J4

During normal operation, the following voltage current readings should be obtained :

Valve	Cathode Voltage	Voltage at Anode Decoupling Point	Screen Voltage
V_8	25V	—	110V
V_5	39V	—	110V
V_7	50V	—	110V
V_9	—	285V	230V
Total anode feed	35mA
H.T. voltage to dividing valves	255V

FRAME DIVIDER
 Technical Description
 M-E.M.I. System of Television
 Item 3.3, April, 1939

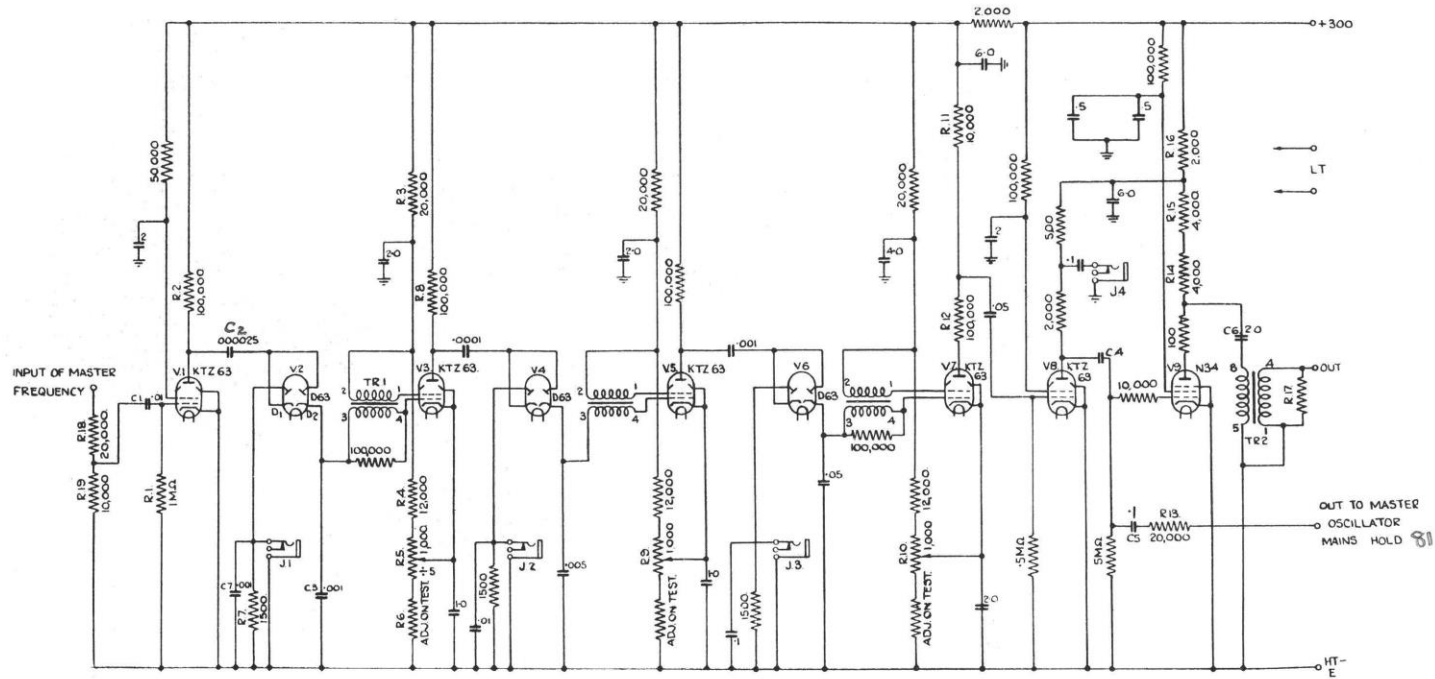


Figure 1. Frame Divider Circuit.

MASTER OSCILLATOR MAINS HOLD

Technical Description

M.E.M.I. System of Television

Item 3.4. April, 1939

to 50 c/s by means of the condensers C_5 and C_6 , and therefore attenuates further any other frequencies not entirely suppressed by $R_3 C_3 R_4 C_4$. The primary is damped by the resistance R_6 , and across this winding therefore we have a sine wave voltage, which we may represent by a single vector, as shown in Fig. 1. From this we must derive an output in 3-phase form, the vector diagram of which is illustrated in Fig. 2. Each of the three phases P_1 , P_2 and P_3 in Fig. 2, are mutually at angles of 120° .

The direct transformation of the waveform of Fig. 1, into that of Fig. 2 would be very cumbersome and impracticable, since to form the new vectors P_2 and P_3 it would clearly be necessary to provide circuits capable of effective phase rotation of $\pm 120^\circ$ in order to derive P_2 and P_3 from P_1 , and unless somewhat complex circuits are to be used it is difficult to obtain a phase angle greater than some 70° or 80° .

The problem is considerably simplified if the single phase output of Fig. 1 is first of all converted into 2-phase form, as illustrated by the vector $P_1 P_1'$ in Fig. 3. For consistency of terminology, the expression 2-phase is used here, but it should be pointed out that there is no difference between the term 2-phase of power engineering and *push-pull* which is more commonly used in circuit phraseology. The transformer TR_1 therefore is provided with a centre tapped secondary, the centre point being connected to earth, and the output across its ends may be directly taken as one of the three push-pull phases. We have now to derive from this output two further push-pull outputs, which we shall designate the vectors $P_2 P_2'$ and $P_3 P_3'$, the phase angle between each set being 120° . It is moreover necessary that the amplitudes of all three vectors should be equal. To see how this is done, reference should now be made to Fig. 4. In this diagram the voltage across the outer ends of the secondary of TR_1 has again been represented by the vector $P_1 P_1'$, and the centre point of the secondary, being earthed, the voltage between one end and earth is represented by the vector OP_1 , and the voltage between the other end and earth by the opposing vector OP_1' . In Fig. 4, using the vector $P_1 P_1'$ as a diameter, the semicircle $P_1' Y P_1$ has been described. Let us choose a point P_2 on the circumference of the semicircle such that the angle $P_2 O P_1$ is 60° . Then the vector OP_2 will represent one side of one of the two push-pull vectors which, to obtain our 3-phase output, we wish to derive from the original push-pull vector $P_1 P_1'$. Now if we join the point P_1' and P_2 , and the points P_2 and P_1 by straight lines, the angle $P_1' P_2 P_1$ will be a right angle, since it is a property of the circle that the angle in the semicircle is a right angle. Now, leaving Fig. 4 for a moment, suppose that, as illustrated in Fig. 5, an alternating voltage E is placed across a condenser and resistance in series, then a current will pass through the circuit, and this will give rise to a voltage E_c across the condenser and a voltage E_r across the resistance. These two voltages E_c and E_r will be in quadrature, that is to say, if represented vectorially then the vectors must be at right angles. The relationship between E , E_c and E_r is shown in Fig. 6. Comparing Fig. 6 with Fig. 4, the vectors E , E_c and E_r of Fig. 6 correspond to $P_1 P_1'$, $P_1' P_2$ and $P_2 P_1$ of Fig. 4. It follows, therefore, that if we were to

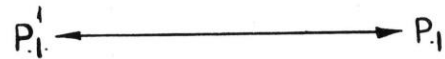


Figure 3

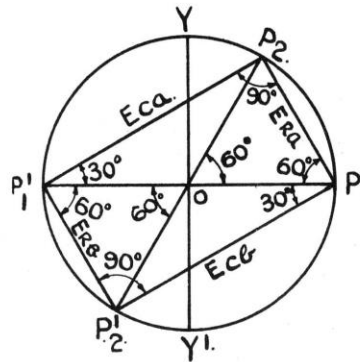


Figure 4

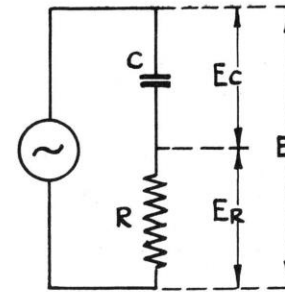


Figure 5

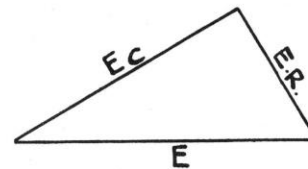


Figure 6

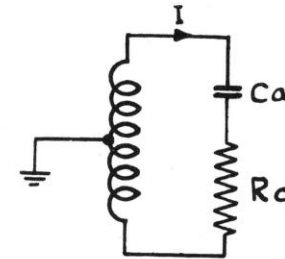


Figure 7

connect a condenser and a resistance in series across the secondary of the transformer TR_1 , as shown in Fig. 7, then if in Fig. 4 $P_1 P_1'$ represents the voltage across the ends of the secondary, then $P_1' P_2$ will represent the

voltage across the condenser, and $P_2 P_1$ will represent the voltage across the resistance. (We may instead elect that $P_1' P_2'$ represents the voltage across the resistance and $P_2 P_1$ that across the condenser, the only difference being that for a given value of resistance and condenser, the position of the point P_2 would be different.) It is evident therefore that the desired phase dis-

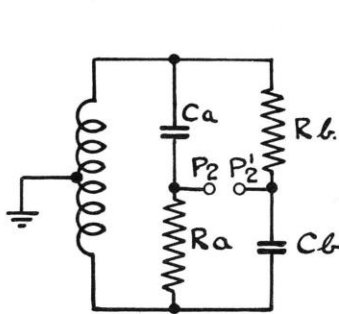


Figure 8

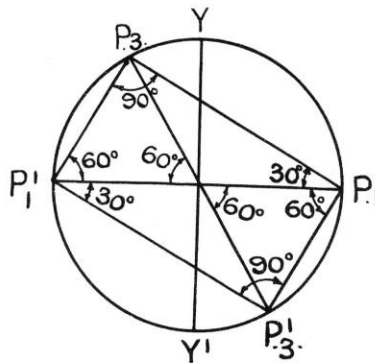


Figure 9

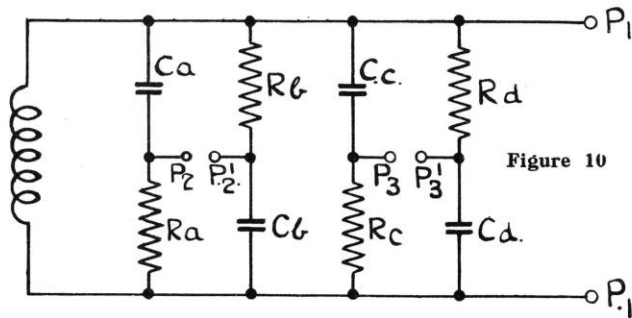


Figure 10

placement between the new vector OP_2 and the original vector OP_1 may be obtained by such a condenser-resistance combination across the secondary. To establish the values of the condenser and the resistance required, we

require to know the phase angle between the voltage across the ends of the secondary and the current I which it sends into the condenser-resistance combination. This current I will be in phase with the voltage which it generates across the resistance, and which is represented in Fig. 4 by the vector $P_2 P_1$. Since the secondary voltage is represented by $P_1' P_1$, the phase angle between it and the current I is the angle $P_2 P_1 P_1'$. Since the angle $P_2 O P_1$ is 60° , the angle $P_2 P_1' P_1$ is, from the properties of the circle 30° , and the angle $P_2' P_1 P_1'$, the phase angle of the current I with respect to the secondary voltage, is 60° , and the elements C_a and R_a must be so chosen as to give this angle. The provision of this pair of elements therefore has provided us with the vector OP_2 at 60° to OP_1 , and of equal amplitude. We now require the corresponding vector OP_2' in push-pull to OP_2 . To obtain this, we complete the lower semicircle $P_1' Y' P_1$ of Fig. 4, and mark the point P_2' so that it is at 180° to OP_2 , i.e., OP_2 and OP_2' are in push-pull. Joining $P_1 P_2'$ and $P_1' P_2'$ we see that, by symmetry, the triangle $P_1 P_2' P_1'$ is identical with the triangle $P_1 P_2 P_1'$, so that for the vector OP_2' we shall require a pair of elements identical with C_a and R_a . It will be seen, however, that in the case of the vector OP_2 , the voltage across the resistance ER_a made an angle of 60° with the vector OP_1 , which is the voltage between one end of the secondary and earth, but in the case of the vector OP_2' , the voltage across the resistance ER_a makes its angle of 60° with the other vector OP_1' , which represents the voltage between the other end of the secondary and earth. This indicates that the position in the circuit of the two elements which are required to provide the vector OP_2' must be reversed with respect to C_a and R_a of Fig. 7. Adding these two elements, C_b and R_b in their correct position, we obtain the circuit of Fig. 8. The complete vector $P_2 P_2'$ therefore appears at the points $P_2 P_2'$ of Fig. 8.

We now require the vector $P_3 P_3'$, which must be at 60° to both the previous vectors $P_1 P_1'$ and $P_2 P_2'$. We therefore repeat the construction of Fig. 4, being careful to preserve the same conventions of drawing, and the construction for $P_3 P_3'$ is shown in Fig. 9. The point P_3 is chosen so that the angle $P_3 O P_1'$ is 60° , and the remainder follows as before. It is evident that two further pairs of elements are required, C_c and R_c , and C_d and R_d , so chosen that they give a phase angle of 30° . Adding these two pairs, we get the circuit of Fig. 10.

The advantage of adopting push-pull outputs was that the phase angles to be given by the phase changing networks do not exceed 60° . Referring to the circuit diagram of Fig. 12, the elements of Fig. 10 can now be recognised. The two 60° combinations shown in Fig. 10 as $C_a R_a$ and $C_b R_b$ are represented in Fig. 12 by $C_8 R_7 R_8$ and $C_9 R_9 R_{10}$. The two 30° combinations shown in Fig. 10 as $C_c R_c$ and $C_d R_d$ are represented in Fig. 12 by $C_{10} R_{11} R_{12}$ and $C_{11} R_{13} R_{14}$.

The vector $P_1 P_1'$ is the output direct across the secondary of the transformer TR_1 , and it is applied to the push-pull amplifier $V_3 V_4$. The output

MASTER OSCILLATOR MAINS HOLD

Technical Description

M-E.M.I. System of Television

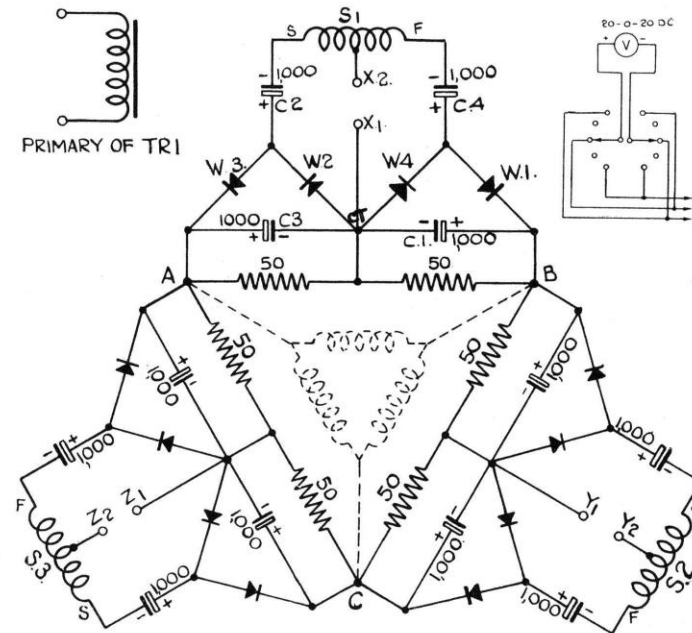
Item 3.4. April, 1939

from the 60° networks, i.e. the vector $P_2 P_2'$, is applied to the push-pull amplifier $V_5 V_6$, and the output from the 30° networks, i.e. the vector $P_3 P_3'$, is applied to the push-pull amplifier $V_7 V_8$. These three amplifiers operate normally except that one valve of each pair shares a common cathode resistance. On one side V_3, V_5 and V_7 share the resistance R_{15} , and on the other side the valves V_4, V_6 and V_8 share the resistance R_{16} . These two common cathode resistances are provided to feed back, and so reduce in amplitude, any out of balance component between the 3-phase, which it would, of course, be undesirable to have in the output. The presence of these cathode resistances, however, results in excessive negative grid bias being applied to the grids of the push-pull amplifiers, but this is obviated by the simple expedient of returning the centre point of the secondary, which is common as regards D.C. to all six amplifier grids, to a suitable point on the H.T. potentiometer $R_{17} R_{18}$, from which an appropriate positive bias is obtained. The push-pull anode outputs from each of the three amplifiers are transformed into non-push-pull or asymmetrical form by means of the three output transformers TR_2, TR_3 and TR_4 , and are supplied to Panel 2. The transformers are tuned to 50 c/s by the condensers C_{12}, C_{13}, C_{14} .

We may now consider Panel 2, the circuit of which is shown in Fig. 11.

The three outputs from Panel 1, shown in Fig. 12 as $X_1 X_2, Y_1 Y_2$ and $Z_1 Z_2$, are applied to the three corresponding pairs of input terminals $X_1 X_2, Y_1 Y_2$ and $Z_1 Z_2$ of Fig. 11. It will be seen that one of each of these pairs of terminals is in each case connected to the centre point of a secondary of the mains transformer TR_1 . The three secondaries are shown as S_1, S_2, S_3 . The primary of the mains transformer is connected to a single phase supply, so that a single phase mains input is mixed with each phase of the 3-phase frame frequency output from Panel 1. The phases of the mains voltages in each of the three secondaries are, of course, identical. Each of the three sets of mixed frame and mains voltages are rectified in voltage doubling rectifiers, and since all three are identical it will be sufficient to consider the action of one of them, that associated with the input terminals $X_1 X_2$. To begin with, imagine that the secondary S_1 is energised, that there is no frame frequency input to X_1 and X_2 , and that these two terminals are short-circuited. Then, during one half of the mains cycle, when the end of the secondary F is more positive than the other end S , the current will flow from F , via the rectifier W_1 , charging the condenser C_1 , and returning to the centre tapping CT . It will also flow from the centre tapping through the rectifier W_2 , charging the condenser C_2 , and returning to the end S of the secondary. On the other half cycle, current will flow from the end S of the secondary, through the rectifier W_3 , charging the condenser C_3 , and returning to the centre tapping. It will also flow from the centre tapping, through the rectifier W_4 , charging the condenser C_4 , and returning to the end F of the secondary. The outer ends of the condensers C_3 and C_1 are connected to the terminals AB , and everything being symmetrical, these two terminals

will be raised to equal D.C. positive potentials. Now assume $X_1 X_2$ unshorted and the frame input from Panel 1 applied. The standing potentials of the terminals A and B will be modified by the presence of this frame input. Assuming in the first place that its frequency is equal to the mains and that



The three windings S_1, S_2 and S_3 are all secondaries of the mains transformer TR_1 .

The three windings shown dotted in centre are the 3 stator windings of the synchronous motor in the Master Oscillator.

Figure 11
Master Oscillator Mains Hold, Panel 2

it is in phase with the mains, and for example assuming further that when the end F of the secondary S_1 is becoming positive and the frame frequency is making the terminal X_2 positive, it can be seen by tracing out the path of the currents that the voltages across C_1 and C_4 will rise, but those across

C_2 and C_3 will fall. The terminal B therefore becomes more positive than the terminal A . If the mains and frame frequencies are identical so that the phase relationship does not change, then this state of affairs will persist, and terminal B will remain more positive than terminal A . The three windings of the synchronous motor in the Master Oscillator are connected in delta across the terminals A , B and C , and for convenience are shown dotted in Fig. 11 although, of course, the motor is not actually part of that unit. Since in our example the terminal B has become positive with respect to terminal A , a current will flow through the stator winding connected across AB . There will, as a result, be a steady stator field in a particular direction, and assuming for convenience that the rotor happens to be in line with it, it will not for the present rotate. Now suppose that the mains frequency changes. The voltage across the secondary S_1 will gradually move more and more out of phase with the frame input across X_1 , X_2 , and in due course, when it has lost phase by 120° , will be momentarily in phase with another of the frame frequency output, for example, with that applied to the terminals Y_1 , Y_2 . In this, the second rectifier circuit, the same series of operations has been proceeding as was described in connection with the other circuit associated with the secondary S_1 , and in the absence of any input, the terminals B and C were at the same D.C. potential, but when the mains momentarily slip into phase with the frame input across Y_1 , Y_2 , the potential of terminal C becomes more positive than terminal B , exactly as formerly B became more positive than A . The second winding of the synchronous motor is connected across BC , and a current now flows in this second winding, and correspondingly less current in the first winding. Since these windings are geometrically at 120° in the motor, the field has clearly rotated through 120° , and the rotor must rotate to this new position. After a further 120° of phase change, the centre of operations moves to the remaining part of the circuit, that associated with the secondary S_3 , and terminal A is more positive than terminal C . The third winding of the synchronous motor is connected across AC , and this winding now carries the maximum current, the position of the stator field rotates once more through a further 120° , and the rotor moves correspondingly. The appearance of peak positive voltages in succession at the terminals A , B and C in this way continues as long as there is any relative phase change between the mains and the frame frequency, and correspondingly the three windings of the synchronous motor are energised in turn, the magnetic effect within the motor being that the field rotates and obliges the polarised rotor to rotate also. As has been explained, the action of the rotor is to modify the Master Oscillator frequency in such a direction as to reduce the discrepancy between the mains and frame frequencies, and the difference eventually disappears.

It will be evident that the inertia of the whole system, comprising the rectifiers and the synchronous motor control, is comparatively great,

so that the frame frequency is brought gradually rather than suddenly into synchronism with the mains.

The voltmeter V enables the three voltages across the output terminals AB , BC and CA to be read. It will be evident that dependent upon phase conditions the standing voltages between these terminals may be either positive or negative, so a centre zero instrument is employed. Since the sum of any three voltages having a 3-phase relationship must, from their vector diagram, be zero, this will be the case with the three voltages read on the voltmeter V . The voltages will, of course, be steady if the mains and frame frequencies are locked, and the potentials at A , B and C are consequently D.C. potentials, and their sum will always be zero, one being positive and the other two negative, or vice versa.

Operation and Maintenance

There are no adjustments to be made on either panel of this apparatus. During normal operation, the following voltages and feeds should be obtained for the valves in Panel 1.

Valve	Cathode Current	Voltage at Anode Decoupling Point	Screen Voltage	Cathode Voltage	Grid Voltage
V_1	—	—	—	0	—
V_2	35mA	250V	250V	48V	0
V_3	22mA	475V	475V	100V	50V
V_4	26mA	"	"	"	"
V_5	24mA	"	"	"	"
V_6	26mA	"	"	"	"
V_7	36mA	"	"	"	"
V_8	24mA	"	"	"	"

The three meter buttons measure respectively the cathode current of V_2 , $V_3 + V_5 + V_7$, and $V_4 + V_6 + V_8$.

V_2	should read	35mA
$V_3 + V_5 + V_7$	" "	80mA
$V_4 + V_6 + V_8$	" "	80mA
Total feed	" "	195mA
H.T. voltage	" "	475V

In Panel 2, with no input from Panel 1, the voltage across each 50 ohm resistance should be 7V. During normal operation, the sum of the voltages read on the voltmeter in each of the three positions of the selector switch should be zero.

MASTER OSCILLATOR MAINS HOLD
 Technical Description
 M-E.M.I. System of Television
 Item 3.4. April, 1939

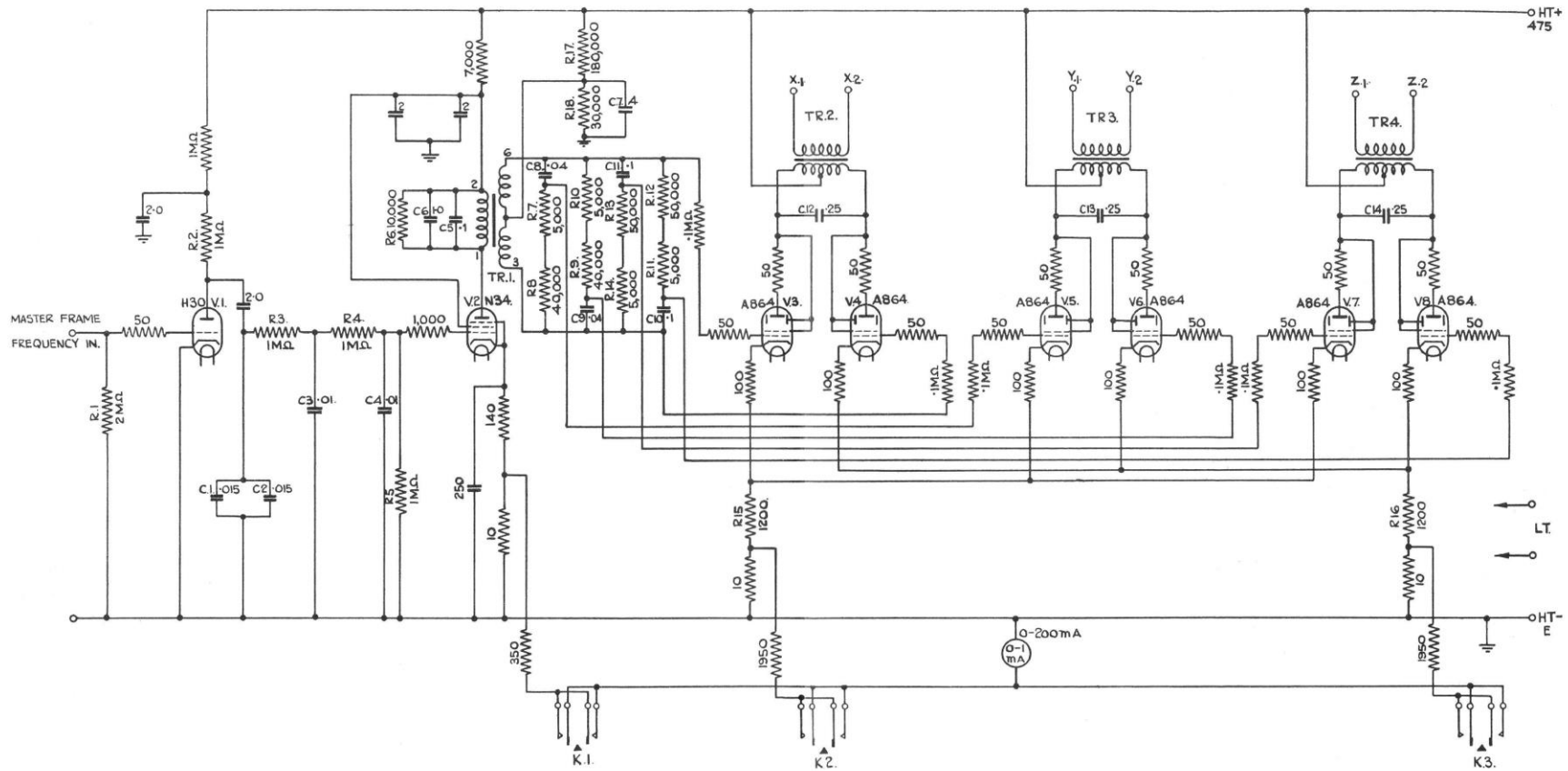


Figure 12
 Master Oscillator Mains Hold, Panel 1.

THE PULSE DELAY UNITS

General

In the sections describing the pulse generators the necessity for the generation and distribution of the various pulses is described. There is, however, one further factor of great importance and that is the time of the arrival of the various pulses at their respective destinations. To cite an example, the sync pulses are injected into the picture and sync mixer, a unit which is

unit. On the left of the diagram are the timing pulse generators providing master frequency, master line frequency and master frame frequency, which provide the timing pulses for the whole system. Where these timing pulse generators supply only one set of camera equipment, for example, one studio, they proceed direct to the apparatus to the right of the vertical line *A-A* in Fig. 1, all of which apparatus is associated with one studio or other picture

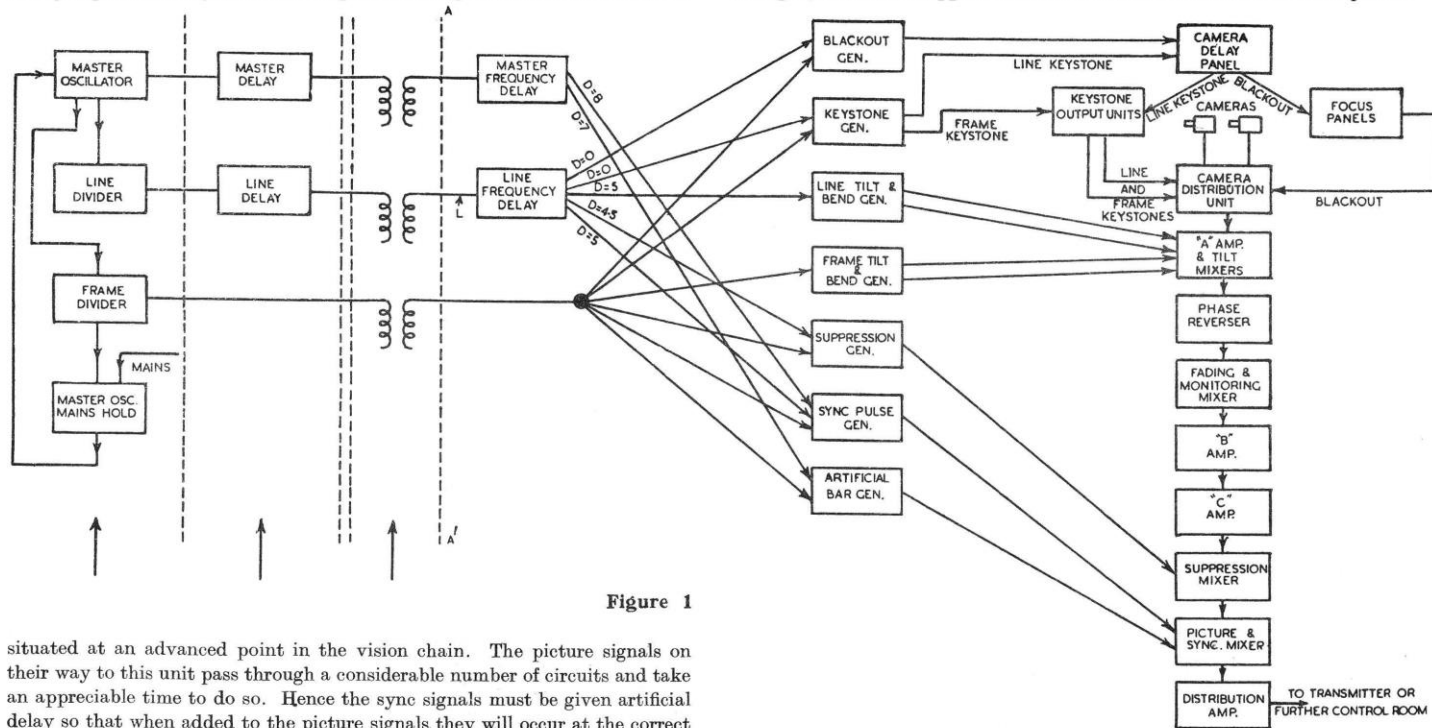


Figure 1

situated at an advanced point in the vision chain. The picture signals on their way to this unit pass through a considerable number of circuits and take an appreciable time to do so. Hence the sync signals must be given artificial delay so that when added to the picture signals they will occur at the correct time. Similar considerations apply to other pulses and it is accordingly necessary to treat the system as a whole and to provide various delay networks to ensure that all the various pulses operate in mutually correct time relationship.

In Fig. 1 is shown a block diagram of the various electronic units with which the camera must be associated in a studio or other picture originating

unit. On the other hand, where a set of timing pulse generators supplies more than one studio, additional units, called the timing pulse distribution delay network, must be inserted. These latter units are described in Section 3.6 and it is the function of this instruction to describe the delay systems associated with local studio apparatus and which will be found in Fig. 1 to the right of the line *A-A'*. These units are the master frequency

suppression and sync pulses the timing of which must be accurately fixed, it at once follows that the first step is to equalise any differences between the times of transmission through the circuits pertaining to individual cameras.

It is not, of course, practicable to accelerate the time of transmission along a camera channel which is employing a long length of cable, and it is accordingly necessary to insert individual degrees of delay into each camera channel, so proportioned with respect to the amount of cable in use that all camera cable circuits will effectively have a transmission time of 4 micro-seconds. For example, if on a production three cameras were being used, camera 1 at the end of 1000 feet of cable, camera 2 employing 500 feet and camera 3 an insignificant amount such as 20 feet, then artificial delay to the extent of 4 micro-seconds would be inserted in the circuit of camera 3, 2 micro-seconds in that of camera 2, and 0 micro-seconds in that of camera 1, and it will be seen that the total delay due to cable plus that deliberately added will in each case amount to 4 micro-seconds.

Clearly the insertion of such a delay may be done wholly in the scanning circuits, or wholly in the vision circuits, or a portion in both, for if it is desired to delay the signal arriving from a given element on the mosaic, it clearly does not matter whether a delay is introduced into the vision signal arriving from that element or whether the scanning is delayed so that that element is scanned later. As obviously the introduction of any apparatus into the vision circuits which could satisfactorily be inserted elsewhere should be avoided, the whole of the delay is placed in the scanning circuits. It is also desirable that the delay to each camera should be individually adjustable so as to be correct for the amount of cable in use at any time with that camera, and it is considered sufficient that the delay should be variable in steps corresponding to the use of 50, 250, 500, 750 and 1000 feet of cable. Since each camera has its own Keystone Output Panel its delay may conveniently be inserted between the Keystone Generator and the Keystone Output Panel, in, of course, the line scanning supply only.

This is achieved by the circuit shown in Fig. 2, in which AB constitutes a network providing the required delay. This network presents some special features of interest. The delay could be produced by a prototype network. It is a property of such networks that the phase characteristic and therefore the constancy of delay introduced with frequency is satisfactory only as far as a maximum frequency equal to half of the cut-off frequency. Such a network would have to be designed therefore with a cut-off frequency of twice the required frequency. It is preferred, however, to use an M -derived network, as such a network gives a uniform delay up to a maximum frequency nearer the cut-off frequency than in the case of a prototype network. Consequently fewer sections can be used. It is desirable to keep the number of sections to a minimum, as any inaccuracy of values of the elements will result in reflections which have very undesirable visual effects in the picture. In the network used, the value of M is 1.3, and requires the insertion of

negative inductances in series with the shunt condensers. Such inductances cannot physically be made, but are effectively produced by coupling together the series inductive sections. Actually the normal method would be to couple all the series elements together to an extent giving a mutual inductance in each case equal to 10% of the self inductance. In such a case all the shunt capacities would have a uniform value but in this case an alternative has been adopted in which some of the series elements are coupled together and a corresponding reduction made in the values of appropriate shunt capacities. The delay introduced by each section is $1/3$ of a micro-second.

It is highly important that the network should be terminated accurately in its characteristic impedance which is, of course, a pure resistance, and this is, according to established network technique, maintained constant over the frequency band by the use of M -derived terminating sections. In this case the network is terminated at both ends, the distant termination involving the M -derived section comprising $L_1 C_1$ and part of L_2 and the final terminating resistance R_1 . The termination at the sending end is actually composed of equivalent elements in the keystone generator, as will be seen from my technical note on that unit. This is done because the nature of the M -derived terminating section does not admit of a shunt capacity, and there will, of course, be a shunt capacity caused by the line between the Keystone Generator and the Camera Delay Unit. Enough, therefore, of the commencement of the filter must be placed in the Keystone Generator so that the particular point at which connection is made from the Keystone Generator to the Camera Delay Unit will occur at the first position in the filter, where there is naturally a shunt capacity. The termination at the sending end is completed by the anode resistance of the last valve of the Keystone Generator. As will be seen from the value of the terminating resistances, the iterative impedance of the network is 2500 ohms. The resistance R_2 is effective in removing a trace of reflection in the higher frequencies.

Along the delay network we therefore have the keystone scanning signal proceeding with increasing delay, and we have to deliver to any Keystone Output Panel the keystone waveform with a selected delay of zero, 1, 2, 3 or 4 micro-seconds, corresponding to the use of 1000, 750, 500, 250 or approximately 0 feet of cable. It may be required to use any number of cameras with the same length of cable, involving the same delay, and this would necessitate paralleling the inputs of as many as six keystone output units upon a point on the delay network giving the required delay. This would, of course, upset the proper value of shunt capacity which should exist in the network at that point, and in addition it would be impossible to keep the capacity constant, as it would vary with the number of keystone outputs connected to it. It becomes therefore necessary to isolate the keystone outputs from the delay network by means of some device which will show the network a very low capacity, and moreover one which does not vary. Clearly a cathode follower is required, and accordingly the valves

PULSE DELAY UNITS
 Technical Description
 M.E.M.I. System of Television
 Item 3.5. October, 1937

V_1 to V_5 are provided. The valve V_1 is connected to the network at a point almost at the beginning where scarcely any delay has been developed, and its input capacity is made up by means of the variable condenser C_2 to the required value of $142 \mu\mu\text{F}$. necessitated by the design of the network at that point.

method of connection, of course, introduces a fixed delay of $1/3$ of a micro-second, which is, however, too small to be noticed.

The valve V_1 therefore supplies the keystone scanning waveform to any camera which is to be used with 1000 feet of cable. The valve V_2 is similarly connected to a point in the network three sections further on, where therefore

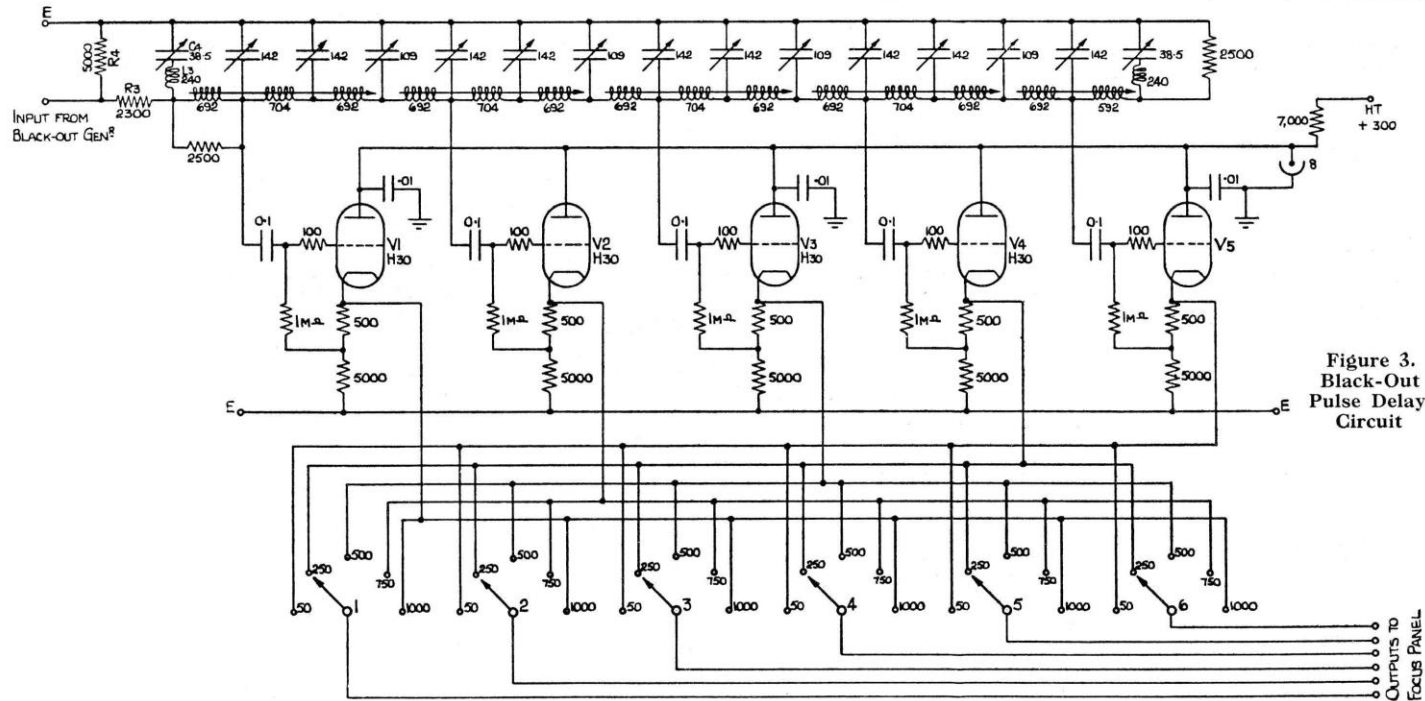


Figure 3.
 Black-Out
 Pulse Delay
 Circuit

Theoretically, of course, the valve V_1 should be connected at the beginning of the network, i.e. across the condenser C_3 , but as indicated above, the total capacity at C_3 consists largely of that of the line from the Keystone Generator to the network, and the actual condenser at C_3 merely makes this up to the required value. If the input to V_1 were placed across C_3 also, this capacity, without any addition, would exceed what is required, and it consequently becomes necessary to feed V_1 from the next section commencing at C_2 , where, there being no other unavoidable capacities except that due to the input of V_1 , the capacity can be made up to the correct value. This

an additional 1 micro-second of delay has been developed, and it will similarly feed all Keystone Output Panels whose cameras are working with 750 feet of cable. The valves V_3 , V_4 and V_5 respectively are connected so as to be appropriate for cameras used with 500, 250 and 0 feet of cable.

The required delay is selected by means of the rotating selector switches S_1 to S_6 , each of which has five positions, one position on each being connected to one of the cathode outputs of the valves V_1 to V_5 . By means of these switches the scanning of any camera can be given the delay appropriate to the length of cable which is being used with it.

We have now to treat in a similar manner the black-out pulses, which are also sent from the Control Room to the cameras. They must, of course, coincide with the return strokes, which latter receive a total delay of $4\frac{1}{2}$ micro-seconds. Clearly the black-out pulses must pass through an identical delay system to that provided for the keystone waveform. This is illustrated in Fig. 3, from which it will be seen that an identical arrangement, comprising the delay network, the five cathode followers and the six selector switches, is provided, and differs only in matters of detail.

In the first place it was necessary in the keystone delay network to put a sending termination in the keystone generator because of the necessity of terminating the network with the utmost accuracy. It will be appreciated that the least reflection caused by an inaccurate termination would affect the velocity of the scanning and produce a most obvious distortion, a distortion comprising errors both of position and illumination, the latter due to velocity modulation effects. In the case of the black-out pulses, however, it is unnecessary to preserve the waveform with such an absolute nicety, as it does not appear in the picture and, so long as it will satisfactorily extinguish the emitron gun beam, no more will be required.

Consequently in the black-out delay network the sending termination, including L_3 and C_4 , may satisfactorily be placed in the camera delay panel, and this is accordingly done. The final sending-end termination, which must consist of the iterative impedance of the network, i.e. a pure resistance of 2500 ohms, is made up partly of the resistance R_3 of 2300 ohms in series with a resistance of 200 ohms formed by the resistance R_4 in parallel with the output impedance of the Camera Black-out Pulse Generator, which is a little over 200 ohms. It is desired that the network shall appear from the point of view of the Camera Black-out Pulse Generator as an impedance of 2500 ohms; without the insertion of R_4 it would appear as 4800 ohms, and the insertion of R_4 gives approximately the correct resistance. Otherwise the network and the associated cathode followers and switches are similar to those provided for the keystone delay.

There is one last adjustment which remains to be made in order that the cameras may satisfactorily operate at the ends of varying lengths of cable. The head amplifier valve heaters are fed from a 22 v. D.C. supply, and adjustment must accordingly be made for the varying amount of resistance introduced by the varying lengths of camera cable. Accordingly six rheostats which maintain the heater current at the correct value, are provided, and situated for obvious convenience in the Camera Delay Unit. These are shown in Fig. 4. In each case the black-out and keystone delay selector switches and the rheostat dealing with one particular camera channel are ganged. There appear on the front of the panel therefore only six controls, one for each camera channel, and each control adjusts simultaneously the keystone delay, the black-out delay and the head amplifier heater current.

The Master Frequency and Line Frequency Delay Units

We may now refer once more to Fig. 1 and consider the general scheme of delays. It will be seen that in addition to the camera delay panel there are two further delay networks, shown as the master frequency delay panel and the line frequency delay panel. Their functions and circuits will now be described.

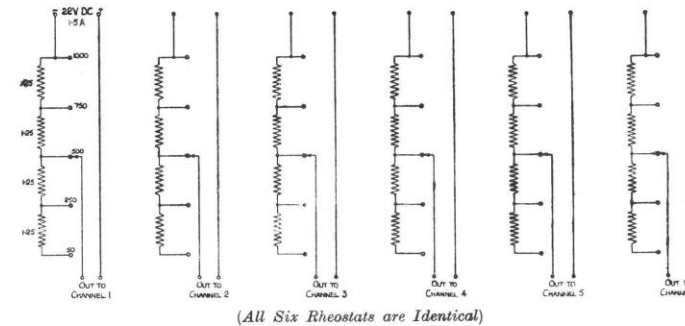


Fig. 4. Head Amplifier Heater Rheostats

We will take as the starting point the time of arrival of a master line frequency pulse at the input to the line frequency delay panel, this point being marked L . The pulse passes through this panel and, amongst other units, energises the Keystone generator which originates the scanning. This passes to the cameras and the picture signal resulting therefrom comes back to the camera distribution unit and thereafter through all the control room units to the distribution amplifier. The total time elapsing between the arrival of a master line pulse at the point L and the arrival of the corresponding point of the generated signal at the output of the distribution amplifier is of the order of 9 micro-seconds, of which 4 are produced as we have seen by the camera delay panel to equalise the delays through all the cameras and picture channels. There is no point in adding to this time, so that the Keystone generator is fed with master line pulses via the line frequency delay panel without any added delay, this being indicated in Fig. 1 by the inscription $D = 0$ against the line input to the Keystone generator. The black-out pulses, having a similar route through the apparatus, are similarly fed with master line pulses at zero delay.

By the time the picture signals have arrived at the A amplifier and tilt mixer there is an accumulated delay of the order of 5 micro-seconds and since tilt and bend pulses are to be injected here they must be similarly delayed; they are therefore fed with master line frequency with 5 micro-seconds of delay added.

PULSE DELAY UNITS

Technical Description

M.-E.M.I. System of Television

Item 3.5. October, 1937

(page re-issued October, 1946)

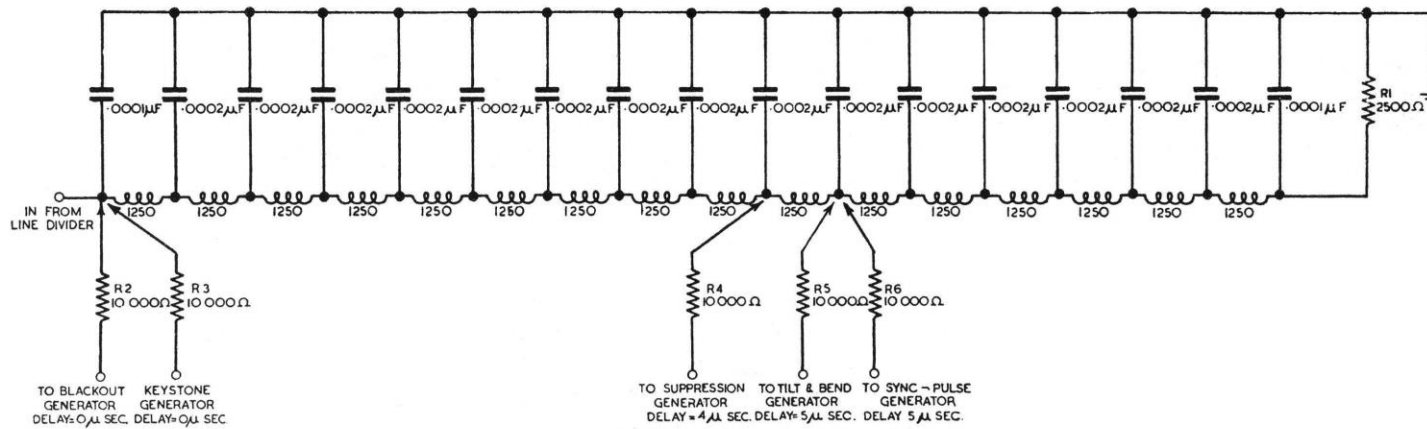


Figure 5. Line Frequency Delay Unit

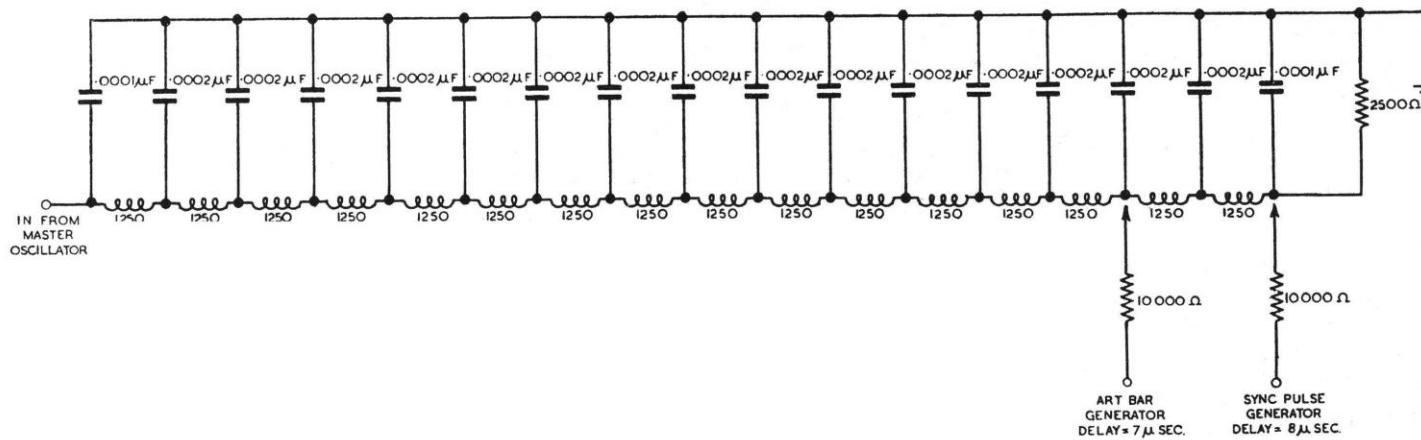


Figure 6. Master Frequency Delay Unit

Coming to the end of the picture channel, the suppression mixer and the picture and sync mixer are at points where nearly the whole of the 9 micro-seconds of delay has accumulated and they are similarly fed with suitably delayed suppression and sync pulses. In these cases, however, the suppression and sync pulse generators will themselves introduce delay and their line inputs are in practice fed with master line frequency at approximately 5 micro-seconds delay.

The sync pulse generator and the artificial bar generator also require inputs at master frequency and they deliver their outputs into the picture and sync mixer where, as has been seen, the accumulated delay will be near its maximum. The operation of the sync pulse and artificial bar generators, however, does not impose so much delay at master frequency as obtains at line frequency. In practice their inputs, which are fed from the master frequency delay panel, are given 8 and 7 micro-seconds delay respectively.

These delays are provided by two identical panels known as the Line Frequency Delay Unit, shown in Fig. 5, and the Master Frequency Delay Unit, shown in Fig. 6. In each case the circuit consists of a simple prototype ladder network having the configuration of a low-pass filter. It is unnecessary in these cases to resort to elaborate m -derived delay networks as the frequency range for purely timing pulses need not be so great as that of the line Keystone pulses.

Considering the line frequency delay unit of Fig. 5, the input consists of master line pulses having a fundamental frequency of 10,125 c/s and a number of harmonics whose amplitudes will in general be inversely proportional to their degree, so that the harmonics become of less importance as their frequency increases. The waveform of the line-timing pulses will be adequately reproduced if some 30 harmonics only are considered, so that the maximum frequency up to which the delay, independent of frequency, is required will be 303,750 c/s ; consequently the cut-off frequency of the

network must be approximately twice this figure. It is actually 640,000 c/s and therefore delay is constant at any frequency between zero and 320,000 c/s. The cut-off frequency is given by the formula.

$$f_c = \frac{1}{\pi \sqrt{LC}}$$

where f_c is the cut-off frequency, L is the value of one of the inductances in henries and C is the capacity in farads of any condenser having an inductance on both sides of it, i.e., any condenser in Fig. 5 except those at the ends of the network.

The network consists of 16 sections, each giving a delay of half a micro-second. This may be calculated by making use of the relation that the delay per second in micro-seconds is equal to the iterative impedance of the network in ohms multiplied by the value of the capacity C , used in calculating the cut-off frequency, in farads. The iterative impedance is given approximately by the formula

$$R = \sqrt{\frac{L}{C}}$$

where R is in ohms and L and C have the meanings given above. (This formula is valueless at frequencies greater than half the cut-off frequency, but, as we have seen, we are not concerned with frequencies of that order.) Alternatively the iterative impedance can usually be found by inspecting the value of the terminating resistance, which in Fig. 5 is the resistance R_1 of 2,500 ohms.

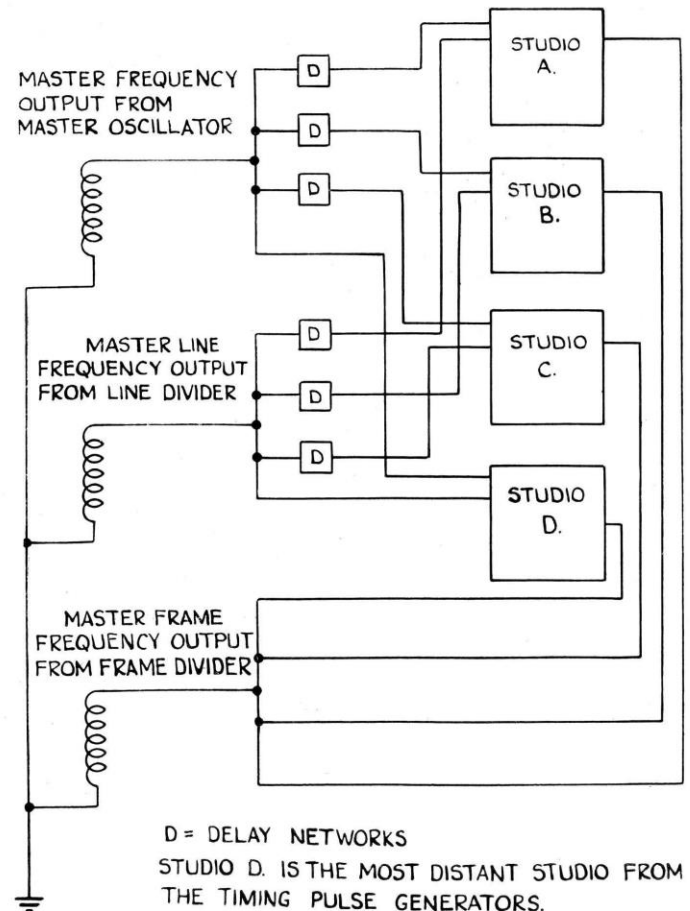
The various outputs are connected to the appropriate points on the networks which will give the desired delay through isolating resistances R_2, R_3, R_4, R_5 and R_6 , all of 10,000 ohms, which prevent the pulse generators fed by the network appreciably feeding back into each other.

The master frequency delay unit illustrated in Fig. 6 is similar in every way and will easily be understood when the design of the line frequency delay unit of Fig. 5 has been appreciated.

THE TIMING PULSE DISTRIBUTION DELAY NETWORKS— MASTER PULSE DELAY, TYPE 1a

Where one set of timing pulse generators is required to feed more than one studio, and the length of line between the former and each of the studios is, as is usually the case, different for each studio, it becomes desirable to insert delay into the lines carrying master frequency and master line frequency to all studios except the most distant one. By this means the propagation times are made equal, irrespective of the distance to any studio, for master and line frequency pulses to pass through the delay networks, the outgoing lines, the control pulse generators and the incoming lines. Thus inter-studio mixing can be carried out if desired. An example of such a layout is shown in Fig. 1, which illustrates a schematic for feeding four studios.

Since the frequency range of both master and line pulses is the same, one type of delay network will suffice for both types of pulses. (No delay



PULSE DISTRIBUTION DELAY UNITS

Technical Description
M.E.M.I. System of Television
Item 3.6. April, 1939
(page re-issued January, 1950)

is required for the master frame frequency.) The circuit of the delay network employed is illustrated in Fig. 2. It consists of five groups of low pass prototype filter sections, G_1 to G_5 , each group having an iterative impedance of 110 ohms and a cut-off frequency of 2.5 Mc/s. The number of sections per group are graded to give various degrees of delay, and each group may

plug P_6 . The outgoing pulses may be monitored by the jack J_1 . The most convenient method of setting up the master frequency and master line frequency networks for any one studio is as follows. Obtain synchronising signals from the most distant studio, and synchronising signals from the studio whose appropriate networks are to be adjusted, and super-

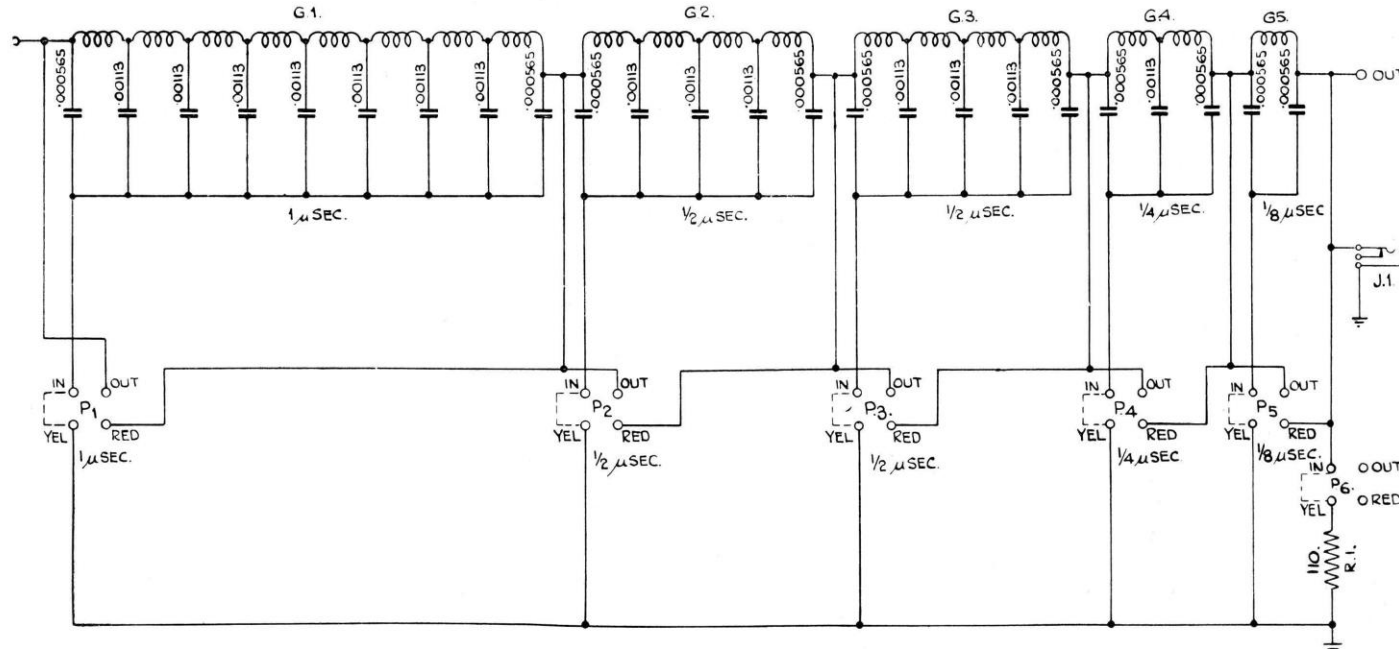


Figure 2. Timing Pulse Distribution Delay Network (Type 1A) Circuit

be cut in or out by means of the five plugs P_1 to P_5 . The delays given by the various groups are as follows:

G_1	..	1 μ sec.	G_3	..	$\frac{1}{2}$ μ sec.	G_5	..	$\frac{1}{8}$ μ sec.
G_2	..	$\frac{1}{2}$ μ sec.	G_4	..	$\frac{1}{4}$ μ sec.			

Each filter has an iterative impedance of 110 ohms, and a cut-off frequency of 2.5 Mc/s, so that its phase response will be linear and its delay constant for all frequencies from 0 to 1.25 Mc/s. If, for any reason, the outgoing line to the studio is removed, the network must be terminated by the equivalent resistance R_1 of 110 ohms, which is inserted by means of the further

impose them on a Waveform Monitor. Adjust the delay of the master line frequency network until exact coincidence between the synchronising signals is obtained. Then set up the same delay on the corresponding master frequency network. It is to be emphasised that *no cameras must be energised* while this adjustment is being made, as when any plug is removed from the delay panel to change the delay, the timing pulses from that panel cease until the plug has been reinserted in a new position, and if cameras were energised their scanning would collapse, with consequent possible damage. The adjustment once made will not require alteration.